CLAIMS

1. A processor system for speech recognition processing of an audio signal, the processor system comprising:

a) front-end processing means for preprocessing of the audio signal and for generating an output of first data,

b) core processing means for performing speech recognition processing on the first data,

c) dual access storage means for buffering of the first data, the dual access storage means being coupled between the front-end processing means and the core processing means,

d) means for invoking the core processing means for performing the speech recognition processing after a time interval following a start of the preprocessing by the front-end processing means,

e) means for stopping the execution of the speech recognition processing by the core processing means when the amount of first data stored in the dual access storage means falls below a predefined threshold level,

f) means for triggering the execution of the speech recognition processing by the core processing means when the dual access storage means is refilled by first data to a level equal to or above the threshold level.

2. The processor system of claim 1 further comprising audio threshold detection means for invoking the front-end processing means when the audio signal surpasses an audio threshold level.

3. The processor system of claim 1 the time interval being a predetermined time interval,

the start of the predetermined time interval being defined by the start of the operation of the front-end processing means and / or by the point of time when the audio signal surpasses a predefined threshold level.

4. The processor system of claim 1 the time interval being determined by a second point of time when the amount of first data being stored in the dual access storage means reaches a second predefined threshold level.

5. The processor system of claim 1 the dual access storage means being a dual ported FIFO or a dual ported RAM.

6. The processor system of claim 1 further comprising clock control means for controlling a first clock signal supplied to the front-end processing means and for controlling a second clock signal supplied to the application program processing means, the clock control means being adapted to invoke the second clock signal the time interval after the first clock signal has been invoked.

7. The processor system of claim 1 the front-end processing means being adapted to calculate a cepstrum and the application program processing means being adapted to perform a speech recognition based on the cepstrum provided by the front-end processing means.

8. The processor system of claim 1, the processor system further comprising:

a) second dual access storage means for buffering of output data being generated by the core processing means by performing the speech recognition processing,

b) back-end processing means being coupled to the second dual access storage means for back-end processing of the output data,

c) means for invoking the back-end processing means after a time interval after a start of the

processing of the application programming processing means.

9. The processor system of claim 8 the time interval being a predetermined time interval.

10. The processor system of claim 8 the time interval being determined by a threshold level of the amount of output data.

11. The processor system of claim 9 further comprising clock control means for controlling a first clock signal supplied to the core processing means and for controlling of a second control signal supplied to the back-end processing means, the clock control means being adapted to invoke the second clock signal the time interval after the first clock signal.

12. The processor system of claim 9 the core processing means comprising speech engine means and the back-end processing means comprising filter means.

13. A method for processing of an audio signal, the method comprising the steps of:

a) invoking of front-end processing means for preprocessing of the audio signal and for generating an output of first data,

b) buffering of the first data in a dual access storage means,

c) invoking of core processing means being coupled to the dual access storage means for speech recognition processing of the first data a time interval after the front-end processing means has been invoked,

d) stopping the execution of the speech recognition processing by the core processing means when the amount of first data stored in the dual access storage means falls below a predefined threshold level,

e) triggering the execution of the speech recognition processing by the core processing means when the dual access storage means is refilled by first data to a level equal to or above the threshold level.

14. The method of claim 13 whereby the time interval is a predetermined time interval.

15. The method of claim 13 the time interval being determined by an amount of first data in the dual access storage means.

16. The method of claim 13 further comprising selectively applying a first and a second clock signal to the front-end processing means and the application program processing means, respectively, for sequentially invoking the front-end processing means and the application program processing means.

17. The method for speech recognition processing of an audio signal of claim 13, the method further comprising the steps of:

a) buffering of second data outputted by the core processing means as a result of the speech recognition processing in second dual access storage means,

b) invoking back-end processing means for back-end processing of the second data after a time interval after the core processing means has been invoked, the back-end processing means being coupled to the second dual access storage means.

18. The method of claim 17 the time interval being a predetermined time interval.

19. The method of claim 17 the time interval being determined by an amount of first data in the dual access storage means.

20. The method of claim 13 further comprising selectively applying a first and a second

clock signal to the front-end processing means and the core processing means, respectively, for sequentially invoking the front-end processing means and the core processing means.